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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,618	06/25/2003	Takanori Tamai	239415US2S	2502

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EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,618	TAMAI, TAKANORI	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-20* is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 4-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 9 is objected to because of the following informalities: In line 13, the word synthesis is misspelled.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Bluemi, "A workbench for generation of component models".

3. As for claim 1, Bluemi disclose a preprocessor, wherein a first circuit description file containing a first hardware description language and a second hardware description language is processed on the basis of a preprocessor control file, and at least a portion described by the first hardware description language in the first circuit description file is converted into the second hardware description language to create and output a second circuit description file [pg. 466-467, section 2.; pg. 467, fig. 1; pg. 469, preprocessor and method modules sections, and fig. 2 – Bluemi discloses a first circuit description wherein the MM transforms ACM and MSI into HDL under control of the preprocessor control file].

4. As for claim 3, Bluemi discloses the second hardware description language includes one of Verilog-HDL and VHDL [pg. 467].

5. Claims 9-20 are allowed over the prior art of record.

6. Claims 2, and 4-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: The prior art of record fails to disclose either singularly or in combination the invention as claimed, including at least [claim 2] a preprocessor, wherein a logic synthesis control script file for a gated clock circuit is further created and output on the basis of the preprocessor control file and the first circuit description file; [claim 4], a preprocessor wherein the processing of the first circuit description file is processing of extracting the first hardware description language from the first circuit description file, converting the first hardware description language into the second hardware description language, and outputting the second circuit description file without converting a portion described by the second hardware description language in the first circuit description file; [claims 5-8], a preprocessor, wherein the first circuit description file includes a description about a flip-flop, which is described by the first hardware description language, and information corresponding a circuit obtained by forming a gated clock the description about the flip-flop converted into the second hardware description language and output; [claims 9-14], an integrated circuit design system comprising preprocessor which processes a first circuit description file containing a description of a flip-flop described by a first hardware description language on the basis a preprocessor control file, creates a second circuit description file by converting at least the description of the flip-flop into a second hardware description language, and creates a logic synthesis control script file a gated clock circuit; [claims 15-20], an integrated circuit design method comprising logically synthesizing circuit description file output from the preprocessor using a logic synthesis control script file for a gated clock circuit and logic synthesis control script file for circuits other than gated clock circuit by a logic synthesis tool to convert the files into a circuit description file using a cell as a basic unit of a circuit and create a netlist.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
April 1, 2005